Performance Results of a Prototype Board Designed for Copper Data Transmission in KM3NeT

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Performance results of a prototype board for copper data transmission

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***Abstract*—The experience gained in designing submarine neutrino telescopes suggested to explore new ways of realizing the data transmission backbone at the detection unit level. In order to decrease the difficulties of integration and handling of the backbones, some effort has been spent in developing a backbone based on copper links with simple tracts of cable connecting contiguous storeys. This work is aimed at the presentation of the general architecture of the system, at the description of an electronic board prototype designed to test the project feasibility with the first results obtained. The main goal of the experimental setup was measuring the recovered clock jitter under various conditions, with and without cables. The jitter measured on the cleaned clock amounts to hundreds of picoseconds, well below the sub-nanosecond time resolution required by this kind of experiments.**

I. Introduction

Lessons learnt from current experiments developing neutrino telescopes, led us to look for new ways of implementing data transmission at the *detection unit* (DU) level. The use of fiber optics in backbones usually implies high cost mainly due to constraints of maintaining the optical power budget. This implies a high cost of cables and connectors, substantial manpower effort for the integration (fiber handling is a delicate operation), the difficulty of testing the integrated system, the power required by electro-optical transceivers and, in the case of DWDM systems, the high price of the transceiver itself. Most of these issues are circumvented through the use of copper links: handling - and hence integration - is much easier, connectors are more common and cheaper than the optical counterpart, while the devices which implement the physical layer of the transmission system are inexpensive. On the other hand, the use of copper links requires a sophisticated implementation of the transmission system, both from a hardware and software point of view.

Recent technological progress, specifically in audio/video data transmission, made available on the market suitable devices capable of transmitting high data rates (many Gb/s) over long distances (hundreds of meters, depending on the medium). The idea behind this paper is to adapt such a proven technology for the purposes of a submarine experiment.

The basic unit of neutrino telescopes can be defined as the DU. The DU consists of many "storeys" vertically distributed in a structure as high as 800 m; each storey hosts photomultipliers (PMTs), usually grouped in 3 to 6 elements. The total number of sensors per DU ranges from 60 to 120. The telescope is far from the shore laboratory, typically it is placed at a depth of thousands of meters and at distances of many tens of kilometers, and produces an amount of data on the order of 1 Gb/s; these constraints require a telescope-to-shore data transmission system based on fiber optics. The data produced by a group of sensors are collected by the storey electronics and routed to on-shore through a DU backbone. The transmission backbone inside the DU has been successfully implemented in optical fibers in NEMO and Antares experiments [1], [2], [3], where DWDM backbones based on Add and Drop modules have been realized.

In Section II the requirements of a copper system will be briefly discussed and, in Section III, both a possible implementation of the general architecture and the prototype board designed to verify the feasibility of the system are presented. After a description of the experimental setup in Section IV, preliminary results measured on the prototype board will be shown. Finally in Section V some conclusions are drawn on the performance of the system and on its applicability.

II. Copper link highlights

The short distances (maximum 50 m) between storeys and the relatively low data rate per storey led us to evaluate a new approach based on copper wires in the DU backbone. The main constraints taken into consideration in the design of a copper backbone were:

- a maximum inter-storey distance of 50 m;
- a reasonable data rate on the link is about 1 Gb/s;
- that the cable should be mechanically manageable;
- that storeys be connected by single tracts of cables.

The data rate over the backbone is highly asymmetrical: data flowing from on-shore to the storeys are for control and setup,

i.e. the data rate can be as low as few hundreds of kb/s per storey. On the opposite direction the data rate must support the transmission of physics data, at least 10 Mb/s per 10" PMT. For both directions we assume that the best (and only choice, if minimization of cable number is required) is to transmit a synchronous bitstream which embeds both clock and data. The low speed of the control channel allows the receiver to recover the clock signal guaranteeing the necessary sub-nanosecond precision required by this kind of experiment.

A low wire count is necessary in order to have a manageable submarine cable. The requirment that storeys should be connected with independent tracts, without signal extraction from the backbone by means of breakouts, aids in this respect: connectors can be realized with a low number of electrical pins.

III. System Architecture

The general architecture of the copper backbone has been already explained in other documents [4]. Briefly, the daisy chain architecture, shown in fig. 1, requires that each node receives the slow serial data stream transmitted by the previous node on the blue link, recovers the clock embedded in the stream, extracts clock and data, *cleans* the clock and uses this de-jittered clock to transmit data to the next node in the chain and to provide the clock reference for transmission in the other direction. Of course, the clean clock is also used to feed each electronic device which needs a reference synchronous to the backbone clock. The Copper Node hosts an FPGA so

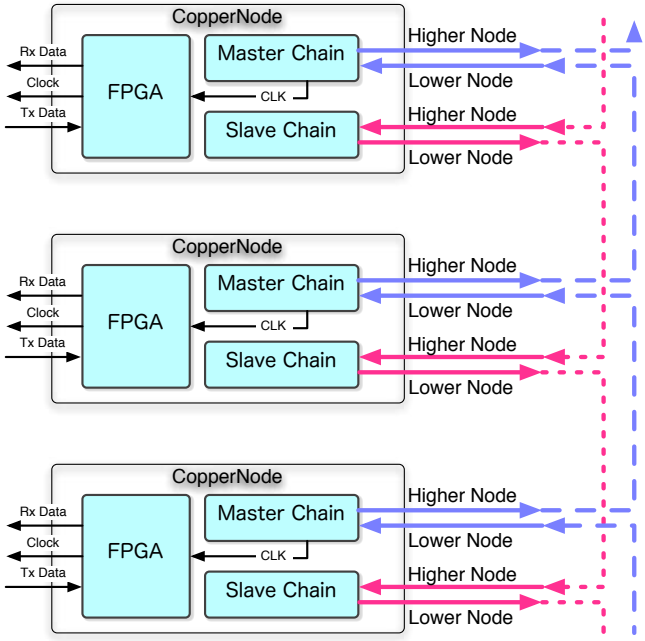

Figure 1. Full Double Daisy Chain architecture.

that the daisy chain mechanism is completely user transparent: each node in the chain has to manage all the data flow and can "add and drop" its own payload; the node appears as a parallel interface to transmit and receive data. There are also controls and clock flags to manage timing issues and handshake protocols.

This document describes the preliminary tests of the reduced Copper Node prototype board, the so called "cNodeV1" board. Actually the cNodeV1 board is a subset of a complete copper node which would be able to provide the required full duplex, asymmetrical full daisy chained communication link on copper media. The cNodeV1 implements only the slow path of the chain: data are serially transmitted at a rate of about 200 Mb/s.

The main goal of the prototype is to demonstrate that the full daisy chain scheme is capable to transmit serially on a copper medium both clock and data, that the *Bit Error Rate* (BER) on data is acceptable, the clock is recoverable, and its quality is still adequate for neutrino experiments. This last requirement imposes a maximum jitter on the clock well below 1 ns. This being the major issue regarding the data transmission on copper, the cNodeV1 board is intended to give an answer to this prolem.

To avoid the constraint to choose in advance a specific transmission cable, i.e. the characteristic cable impedance, the line interface has not been embedded on the board. Instead, use of high speed SMA connectors allows to change both the line driver and equalizer and also the cable. Moreover we do not address here the problems concerning either the impedance change, due to the high pressure in the submarine environment typical of a neutrino telescope, or the behavior of the system with real submarine connectors. Figure 2 shows a block diagram of the cNodeV1 board with the line interface.

IV. Experimental Setup

The cNodeV1 can be plugged into a Xilinx ML50x evaluation board using an adapter already developed for another application: this configuration is shown in fig. 3. For the tests we used both a ML507 board, which hosts a Virtex-5 FX FPGA with a hardwired embedded PowerPC processor, and a ML505 board, where a MicroBlaze embedded processor has been synthesized in the Virtex-5 LX FPGA.

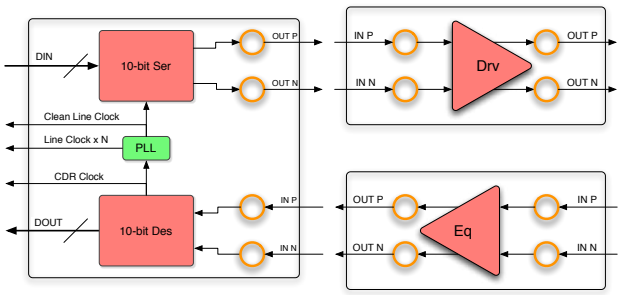

Figure 2. Block diagram of the *Master Chain* block shown in fig. 1. Also the line interface is present with a cable driver and an equalizer.

To measure the BER, a dedicated module has been specifically written: the FPGA transmits a sequence of random bytes, coded according to 8b10b protocol, to the transmitter which serializes them; after the cable, the stream is received by the receiver, de-serialized and passed back to the FPGA. After

an initial phase, the FPGA logically locks onto the received stream and transmitted data are compared against received data: in case of errors a counter is incremented and updated each second.

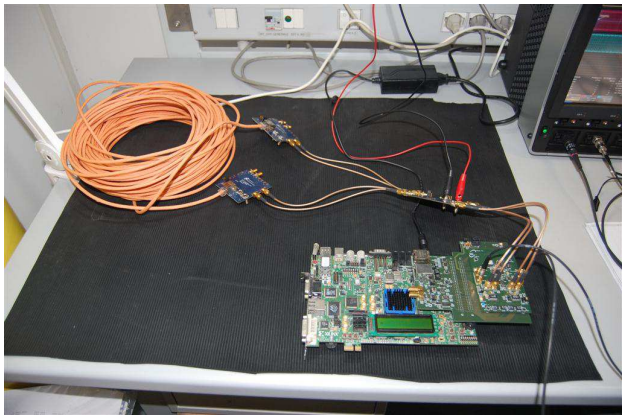

Figure 3. Experimental setup with the cNodeV1 board plugged into the ML505 board through the adapter. The line driver transmits the signal through a CAT5e cable 30 meters long and the signal is received by the cNodeV1 receiver after the equalization.

A program has been written to manage the system: the cNodeV1 board can be intialized, the BER module can be switched on and off or reset, errors on the transmission can be forced to check if the BER measure is effective[1], and the BER results can be read by the processor. A simple RS232 connection is used for the communication.

All the measures have been taken using a LeCroy SDA Zi760, with 6 GHz of bandwidth and 40 GS/s of sampling rate. This instrument is specifically designed for serial data analysis allowing the user to extract bitstream feature and characterizing the clock performance of the system independently from the receiver.

A. Single hop setup

The single hop configuration consists of one cNodeV1 board plugged into an ML505 board. Fig. 4 schematically shows the block diagram of the system. The clock used for transmission is a local 16.384 MHz oscillator. The receiver, using an internal Clock and Data Recovery (CDR) module, extracts from the stream both clock and data, which are acquired by the FPGA. The recovered clock is also fed to the PLL which provides a synchronous and clean version of it.

In the next Sections the results obtained under different line conditions will be analyzed.

1) Single hop with coaxial cables pair: In this configuration data are transmitted to the receiver through high speed coaxial cables pair 20 cm long without inserting any driver or equalizer: this is the best possible condition which gives us an idea of the minimum jitter value attainable. The waveforms of the source clock and of the clocks before (CDR Clock) and after the PLL (Clean Line Clock) have been sampled to measure the Time Interval Error (TIE)[2] quantity.

[1]This is particularly useful when the link is too good to show errors in a reasonable time

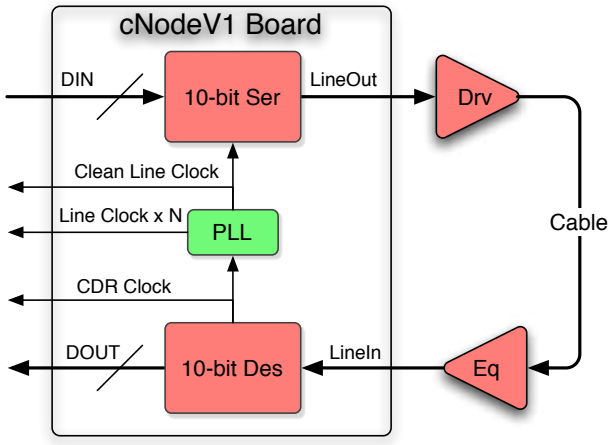

Figure 4. Single hop block diagram: the cNodeV1 board, plugged into the host board, drives the cable and receives back the data.

The standard deviation of the TIE for the source clock is about 340 ps; even in this optimal case the TIE of the recovered clock before been cleaned has a standard deviation of 450 ps while, after applying the PLL, the jitter is reduced down to 10 ps.

2) Single hop with 2 m long CAT5 cable: With this setup, a CAT5 cable 2 m long has been inserted between the line driver and the receiver; the TIE standard deviation of the clock cleaned by the PLL is slightly worse than what we found previously in Section IV-A1 but it is still very good being about 13 ps for the clean clock. The TIE of the recovered clock is now 500 ps due to the longer cable.

3) Single hop with 30 m long CAT5e cable: The same performance values have been evaluated using a CAT5e cable 30 meters long. The TIE standard deviation for the clean clock is still about 15 ps, while the value for the recovered clock increased up to 550 ps.

B. Double Hop setup

In the double hop configuration depicted in fig. 5 we have one cNodeV1 prototype board plugged into the ML505 board and a second cNodeV1 which, plugged into the adapter, can work in a stand-alone fashion. Data are transmitted by the first node to the second which recovers the clock, cleans it by means of the PLL and retransmits data back to the first node which, in turn, recovers and cleans the clock. Measures are made to assess system synchronicity and clock jitter.

1) Double hop with 300 m long CAT5e cable and short coaxial cables: In the examined configuration, the first hop uses a 300 m long CAT5e cable with a driver and equalizer pair; the second hop is covered by 2 high speed coaxial cables 1 m long without any driver or equalizer.

[2]The TIE is a first rough measure of the jitter: it represents the distance between the edges of the acquired clock and the expected edges inferred from the clock itself. See for example [5]

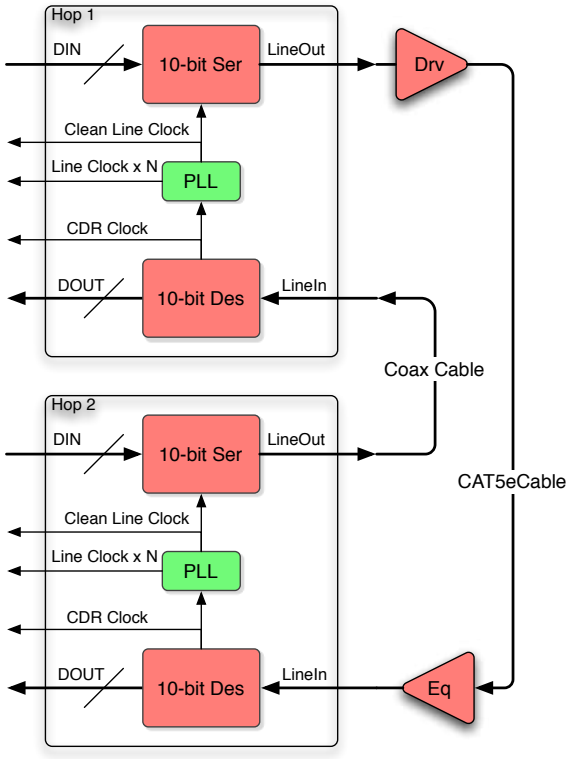

Figure 5. Double hop block diagram: the first hop consists of a cNodeV1 plugged into the ML505 board and acting as the chain source. The second hop is implemented with a cNodeV1 board working stand-alone. The driver and equalizer pair are inserted only in the path between first and second node.

Each node recovers the line clock and cleans it by means of its own PLL: the clock from the first node shows a standard deviation of the TIE of about 19 ps while the clock from the second node has a value of 37 ps. The mean period for the two clocks is the same: 61.03563 ns (calculated over about 8 million time windows 50 μs each) with a standard deviation of 6 ps and a maximum peak-to-peak deviation of 90 ps. This confirms that the two nodes are synchronous and the instantaneous deviation is small.

C. Jitter analysis performed by SDA analyzer

We tried also to estimate the BER on data letting the SDA analyzer do the job for us. We transmitted the random data on the 300 m long CAT5e cable using both driver and equalizer; then the two differential signals driven by the equalizer were read by the instrument and subtracted to yield the single ended serialized stream. Fig. 6 shows the jitter analysis performed on this signal: the eye diagram at a BER value of 10^{-12} is still open by a 20 % of the unit interval, as extrapolated in the bathtub curve. The TIE time evolution does not exhibit any evident trend and the TIE histogram looks gaussian, stressing that there are no deterministic jitter components. The estimated total jitter on the signal is less than 4 ns. The clock extracted from the stream will be cleaned using the PLL to provide the performance stated in IV-B1.

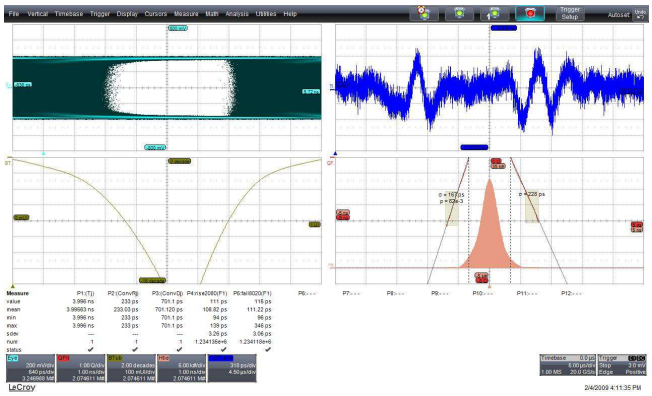

Figure 6. Jitter analysis provided by the LeCroy SDA instrument: the line differential signals after the driver and equalizer pair and a CAT5e cable 300 m long are analyzed.

V. Conclusion

The preliminary results shown in this paper are very encouraging: the transmission of a 200 Mb/s stream on a CAT5e cable seems feasible even over distances longer than 300 m. Data received show a low BER value; the clock can be extracted from the serial stream and, after a cleaning step implemented by a PLL, the jitter is reduced to tens of ps. The tests used only two hops, but in the near future a higher number of boards will be cascaded to check the performance of a longer chain.

The effects of change in cable impedance due to the pressure of submarine environment coupled with the use of inexpensive connectors - not normally deemed suitable for use with fast differential signals - will be analyzed in the near future using a hyperbaric chamber and a setup based on commercial cables and connectors. Since the maximum distance between adjacent storeys is expected to be 50 m, we are optimistic that the performance at high pressures will be similar to that measured in this work, using standard connectors and cables within the 300 m length already studied.

Acknowledgments

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